Atomic Scale Interface Analysis with MEIS for Nano-Electronics Technology

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It was shown that MEIS can provide reliable thickness measurement of nm gate oxides down to 1~2 nm range with additional interface strain profiles which show interesting correlations with electrical properties. Its absolute quantification capability with atomic layer depth resolution can be utilized to develop delta doped reference thin films especially for SIMS shallow junction profiling. It was discussed that MEIS has quite high potential to contribute to the further development of nm ultrathin films with atomic resolution to meet the challenging and urgent demands from nano-electronics technology.

1. Introduction

With the continued shrinkage of CMOS device dimension, the demand on nm ultrathin film characterization has reached to the point that atomic scale information on atomic layers in ultrathin films is required from the top surface layer to the bottom interface layer on the substrate and even beyond. According to the ITRS road map [1], the equivalent thickness of gate oxides is less than 1nm and that of shallow junction is less than 10 nm in 35 nm technology node. The spatial resolution required for gate dielectrics and shallow junctions is in the sub atomic level beyond the present analytical capability and in the range where any physical meaning can be hardly given. What we can do to meet this very challenging and urgent demand from the semiconductor industries is probably approaching the atomic resolution limit and correlating the atomic scale analysis results with the electrical properties, on which the device performance is based on.

To get atomic scale resolution, non-destructive analysis techniques must be employed. There are a few non-destructive surface and interface analysis tools that are useful and promising to meet the above challenges such as Scanning Tunnelling Microscopy, Scanning Transmission Microscopy, angle-resolved X-ray Photoelectron Spectroscopy and etc. Medium Energy Ion Scattering Spectroscopy (MEIS) has been quite successful to investigate the composition and atomic structure of ultrathin films with atomic layer depth resolution non-destructively. In this report, recent MEIS results on analysis of nm gate oxides and delta doped layers will be summarized from points of view as developments of new references and novel new interfacial analysis techniques. For nm gate oxides, comparative studies on the thickness of nm gate oxides down to < 2 nm with MEIS, TEM, ellipsometry and I-V/C-V will be

reported. Interface composition and strain studies for thermal oxide, oxynitride, ozone oxides, and thermal oxides on vicinal Si(100) will be summarized. To tackle the delta doped reference thin films especially for SIMS shallow junction profiling, delta doped Si multi-layers were grown and analysed with MEIS. Present status and future requirement of ultrathin film analysis for nano-electronics are discussed.

2. Experiments

The MEIS analysis for energy spectra was done with 100 keV H^+ incident along the [111] direction and exiting along the $[00\bar{1}]$ direction with the scattering angle of 125° to eliminate the back-scattering signal from crystalline Si(100) substrates. The minimum in the angular distribution of scattered ions corresponds to the bond angle with neighbour atoms due to the blocking mechanism.[2] For blocking dip analysis in MEIS, a 100 keV H^+ beam was aligned slightly off from the $[00\bar{1}]$ direction in the (011) plane, and H^+ scattered from Si atoms in the [111] direction were analysed. The angular resolution determined mainly by the incident ion beam divergence and the 2-dimensional position sensitive detector, was estimated to be about 0.1°. Details of the MEIS techniques and the system used in this experiment are given elsewhere [2,3].

For gate oxide thickness determination studies, gate oxides in the range of 2-9 nm on 8-15 Ω cm P-type wafers were fabricated with furnaces by wet oxidation and catalytic wet oxidation. A native oxide was also measured as one of the gate oxides. The measured oxide thickness on a silicon wafer is uniform within 0.15 nm from ellipsometric analysis for all the samples used in this analysis. The surface is very flat with the root mean square roughness value below 0.1 nm by Atomic Force Microscopy.

All the As delta multiple-layered Si thin films used for this work were grown by an ultra-high vacuum (UHV) ion-beam-sputter-deposition (IBSD) system with *in-situ* MEIS analysis capability and characterized with HRTEM, MEIS, and SIMS. As delta multi-layered Si thin films were grown on *n*-type Si (100) wafers at room temperature by sputtering a Si wafer target. To minimize the As surface segregation during thin film growth, H was dosed to passivate the surface. To determine the amount of As and the thickness of one As delta layer, HRTEM and MEIS was used. For the analysis of the absolute areal density of As atoms for each layer with MEIS, the MEIS system calibration factor was determined using various standards such as Si (100) and Pt (111) surface peak, nm SiO_2 and Ta_2O_5 thin films on Si (100) [4].

3. Results

3.1 Thickness determination of nm gate oxides

As the thickness of gate oxides approaches 1-2 nm, the demand on reliable thickness measurements has been increased. We used MEIS and HRTEM with electrical methods for accurate measurement of gate oxide thickness. In MEIS analysis, we can estimate the gate oxide thickness from the full width at half maximum (FWHM) values of the silicon and oxygen peak. As can be seen clearly in Fig.1, the Si peak is wider than the O peak. The thickness determined by the Si MEIS peak is ~ 1.2 nm thicker than that by the O MEIS peak for the whole thickness range in this work. The main reason is that the interfacial Si atomic layers in the Si substrate below the SiO_2 layer is visible in the double alignment condition. The Si lattice distortion due to the compressive strain present near the SiO_2-Si interface [3] can be additional factor for the Si peak broadening. Therefore, the thickness of gate

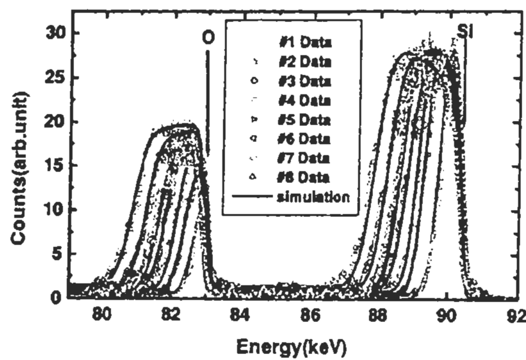

Fig.1 MEIS spectrum of thermal oxide layers on Si (100) taken by 100 keV protons in the double alignment condition with the scattering angle of 125°.

oxides in this work was obtained from the FWHM of Si and O peak and the average values of the energy loss in silicon oxide, 109± 4 eV/nm determined with TEM.

From the areal density of O from the simulations using the ion scattering analysis program [5], the thickness of gate oxides can be calculated with the bulk density of SiO_2 ($6.6x10^{22}$ cm^3). The thickness of gate oxides estimated with ion scattering analysis programs [5] is in a good agreement with that estimated with the FWHM of O MEIS peak.

All of the oxide thickness obtained by several other techniques such as high resolution transmission electron microscopy, spectroscopic ellipsometry, and I-V/C-V are plotted with respect to the thickness based the MEIS simulations as shown Fig. 2. The thickness based on the MEIS simulations is chosen as a reference. The thickness based on the FWHM of MEIS Si peak is always thicker by ~1.2 nm than those of MEIS O peak as shown in Fig.1. It can be noticed that the thickness based on TEM images of completely amorphous SiO_2 layer is very close to that of MEIS O peak within 0.1 nm for the whole thickness range. The good agreement could be a direct result of the procedure that the electronic stopping power in SiO_2 layers is determined by the FWHM's of MEIS O peaks and TEM images of amorphous SiO_2 layer. However, TEM is an extremely local probing tool in contrast to MEIS, of which the analyzed area is quite broad as mentioned above. Considering the many orders of difference in the analyzed area, the good agreement within 0.1nm over the whole thickness range indicates the level of consistency and reliability in the gate oxide thickness determined by MEIS and TEM.

It is quite interesting that the thickness based on the FWHM of MEIS Si peaks is close to that based on TEM images including the inter-layers. The MEIS Si peak width

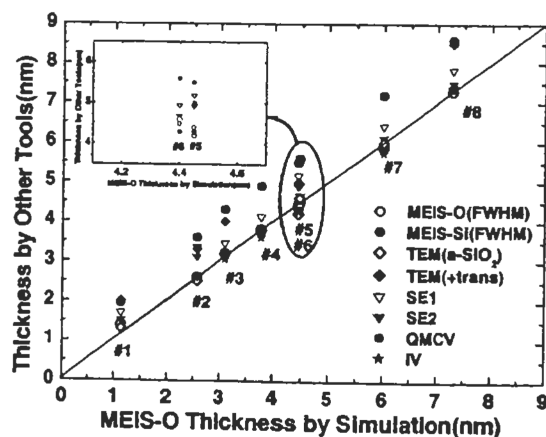

Fig.2 Plots of thickness measured by MEIS, spectroscopic ellipsometry, QM C-V analysis, I-V analysis, and TEM with respect to simulated SiO_2 film thickness.

includes the contributions from a couple of Si interfacial layers in the Si substrate with additional effects due to the Si lattice distortion in the SiO_2-Si interface, which is about 1nm thick.[3] The good agreement between the thickness based on MEIS Si peaks and TEM images of amorphous SiO_2 including the interlayer suggests that the partially disordered layer observed at the SiO_2-Si interfaces in TEM images correspond to the interface layer observed with MEIS. The SiO_2-Si interface consists of SiO_x and Si crystallites, in which the x varies from o to 2 according to the MEIS results.[3]

The electrical thickness of gate oxides based on IV & CV measurements follows closely the physical thickness based on MEIS O peak and TEM images of amorphous SiO_2 layers for the whole range within 0.3 nm except the native oxides. For native oxides, IV and CV measurements were not possible due to the severe leakage current.

3.2 Interface strain profiling in gate oxides

Scaling of metal-oxide-semiconductor field-effect-transistors device dimension require high quality ultra-thin gate dielectric films to satisfy the requirement of reliability characteristics and short channel effect. However, considering the existence of a transition layer at the SiO_2/Si interface, the ultrathin oxide layer is no longer homogeneous.[3,6] Recently, it has been reported that the reliability characteristics of ultrathin gate oxides heavily depend on the SiO_2/Si interfacial stress which was generated due to the volume expansion during thermal oxidation.[6-8]

We previously reported relationship between the oxide structural property and the oxide electrical characteristic.[7] In this paper, using MOS capacitor with ultra-thin gate dielectric grown on 4 degree-tilted wafer, we found a direct correlation between the improvement of reliability characteristics with over an order of magnitude longer device lifetime and the relaxation of the interface strain [9], which was confirmed by MEIS as shown in Fig. 3. Ultra-thin gate dielectric grown on tilt wafer is promising alternative for gate dielectric application of future MOS device.

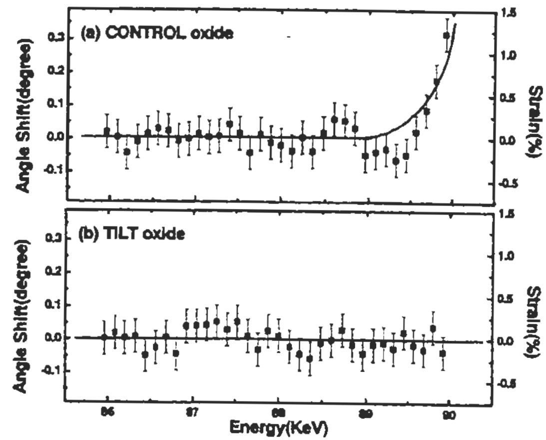

Fig.3. The shift of the blocking dip positions of Si peak as a function of depth for (a) control oxide, (b) tilt oxide in the [111] direction.

3.3 MEIS Analysis of As delta-layers in Si as a SIMS reference thin film

SIMS quantification and depth scale calibration has been based on ion-implanted standards. [10] In this work, the feasibility of using multiple delta-layer reference materials for quantitative SIMS depth profiling is tested and presented. Multiple As

delta-layer Si thin films were made by UHV-ion beam sputter deposition and characterized with HRTEM, MEIS, SIMS. MEIS results in Fig.4 shows that the thickness of As delta layer is less than 1 nm. The interval between As delta layers in the range of 10nm~90nm is determined by HRTEM and MEIS, which can be used to calibrate the SIMS depth scale. The sharp SIMS peak shape of each delta layer is more convenient and useful for precise determination of peak positions compared with rather broad peaks of ion-implanted standards. It was tried to determine the absolute areal density of As atoms for each layer with MEIS based on MEIS system calibration using various standards such as Si (100) and Pt (111) surface peak, nm SiO_2 and Ta_2O_5 thin films on Si (100)[4]. The uncertainty of the areal density determination with MEIS is around 10%.

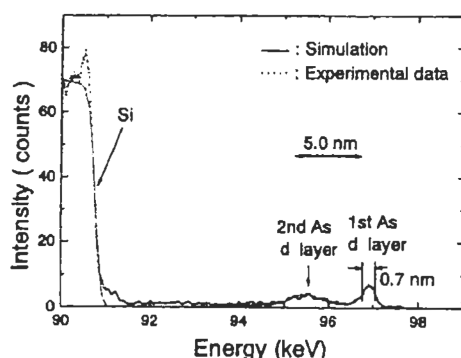

Fig.4. MEIS spectra of an As delta multi-layered Si thin film. 100 keV H^+ ions were incident in the [111] direction and the ions scattered in the [001] direction were measured. The thin film specimen structure is Si(100)/{Si(30nm)/As(1nm)} * 4/ Si(5nm) / As(1nm).

RSF factors determined with the As delta-layer and conventional ion implanted standards are in a good agreement within 10%. With delta-layers present in pre-equilibrium region, it can be proposed to measure the surface transient sputter rate change and probably the RSF factors in the pre-equilibrium region.

4. Conclusions

To meet the challenging demand on atomic scale analysis of nm ultrathin films, MEIS can be one of the useful tools for ultrathin gate oxides and shallow junction analysis. It was shown that MEIS can provide reliable thickness measurement of nm gate oxides down to 1~2 nm range with additional interface strain profiles which show interesting correlations with electrical properties. Its absolute quantification capability with atomic layer depth resolution can be utilized to develop delta doped reference thin films especially for SIMS shallow junction profiling. With complementary use of other practical surface analysis tools such as low energy SIMS and angle resolved XPS, it may be insisted that MEIS has quite high potential to contribute to the further development of nm ultrathin films with atomic resolution to meet the challenging and urgent demands from nano-electronics technology.

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